ABSTRACT OF THE DISCLOSURE

A frequency-voltage mechanism for power management including first and second PLLs, select logic, control logic, and voltage control logic. The first PLL generates a first source clock signal at a first frequency based on a bus clock signal. The second PLL generates a second source clock signal at a second frequency based on a first frequency control signal and the bus clock signal. The select logic selects between the first and second source clock signals to provide a core clock signal based on a select signal. The clock control logic detects power conditions via at least one power sense signal, provides the first frequency control signal according to power conditions, and provides the select signal. The voltage control logic adjusts the operating voltage commensurate with frequency of the core clock signal. Power consumption is dynamically adjusted without undue delay while providing significant power efficiency benefits.